Amendments to the Specification

Please amend the second paragraph on page 13, as below:

- 40, a layer of under bump metal created overlying the pillar metal 38 of the solder bump, wherein ~~the~~ an horizontal distance between an edge of the under bump metal layer and an edge of the metal pillar of the solder bump is greater than 0.2 microns, wherein the layer 40 of under bump metal is an electroplated nickel layer with a thickness between 1 and 10 micrometers.

Please add the following paragraphs between lines 10 and 11 on page 13, as below:

In a typical application insulating layers, such as silicon oxide and oxygen-containing polymers, are deposited using Chemical Vapor Deposition (CVD) technique over the surface of various layers of conducting lines in a semiconductor device or substrate to separate the conductive interconnect lines from each other. The insulating layers can also deposited over patterned layers of interconnecting lines, electrical contact between successive layers of interconnecting lines is established with metal vias created in the insulating layers. Electrical contact to the chip is typically established by means of bonding pads or contact pads that form electrical interfaces with patterned levels of interconnecting metal lines. Signal lines and power/ground lines can be connected to the bonding pads or contact pads. After the bonding pads or contact pads have been created on the surfaces of the chip, the bonding pads or contact pads are passivated and

electrically insulated by the deposition of a passivation layer over the surface of the bonding pads. A passivation layer can contain silicon oxide/silicon nitride (SiO_2 /Si_3N_4) deposited by CVD. The passivation layer is patterned and etched to create openings in the passivation layer for the bonding pads or contact pads after which a second and relatively thick passivation layer can be deposited for further insulation and protection of the surface of the chips from moisture and other contaminants and from mechanical damage during assembling of the chips.

Various materials have found application in the creation of passivation layers. Passivation layer can contain silicon oxide/silicon nitride (SiO.sub.2 /Si.sub.3 N.sub.4) deposited by CVD, a passivation layer can be a layer of photosensitive polyimide or can comprise titanium nitride. Another material often used for a passivation layer is phosphorous doped silicon dioxide that is typically deposited over a final layer of aluminum interconnect using a Low Temperature CVD process. In recent years, photosensitive polyimide has frequently been used for the creation of passivation layers. Conventional polyimides have a number of attractive characteristics for their application in a semiconductor device structure, which have been highlighted above. Photosensitive polyimides have these same characteristics but can, in addition, be patterned like a photoresist mask and can, after patterning and etching, remain on the surface on which it has been deposited to serve as a passivation layer. Typically and to improve surface adhesion and tension reduction, a precursor layer is first deposited by, for example, conventional photoresist spin coating. The precursor is, after a low temperature pre-bake, exposed using, for example, a step and repeat projection aligner and Ultra Violet (UV)

light as a light source. The portions of the precursor that have been exposed in this manner are cross-linked, thereby leaving unexposed regions (that are not cross-linked) over the bonding pads. During subsequent development, the unexposed polyimide precursor layer (over the bonding pads) is dissolved, thereby providing openings over the bonding pads. A final step of thermal curing leaves a permanent high quality passivation layer of polyimide over the substrate.

Barrier layers, such as layer 36, are typically used to prevent diffusion of an interconnect metal into surrounding layers of dielectric and silicon. Some of the considerations that apply in selecting a material for the barrier layer become apparent by using copper for interconnect metal as an example. Although copper has a relatively low cost and low resistivity, it has a relatively large diffusion coefficient into silicon dioxide and silicon and is therefore not typically used as an interconnect metal. Copper from an interconnect may diffuse into the silicon dioxide layer causing the dielectric to be conductive and decreasing the dielectric strength of the silicon dioxide layer. Copper interconnects should be encapsulated by at least one diffusion barrier to prevent diffusion into the silicon dioxide layer. Silicon nitride is a diffusion barrier to copper, but the prior art teaches that the interconnects should not lie on a silicon nitride layer because it has a high dielectric constant compared with silicon dioxide. The high dielectric constant causes a desired increase in capacitance between the interconnect and the substrate.

A typical diffusion barrier layer may contain silicon nitride, phosphosilicate glass (PSG), silicon oxynitride, aluminum, aluminum oxide (Al_XO_Y), tantalum, Ti/TiN or Ti/W,

nionbium, or molybdenum and is more preferably formed from TiN. The barrier layer can also be used to improve the adhesion of the subsequent overlying tungsten layer.

A barrier layer is preferably about 500 and 2000 angstrom thick and more preferably about 300 angstrom thick and can be deposited using rf sputtering.

Please amend the sixth paragraph on page 14, as below:

- 54, the pillar metal of the interface between the device 50 and the BGA substrate 52, similar to pillar metal 38 of FIGS. 3 and 4, wherein the pillar metal 38 or 54 is an electroplated copper layer with a thickness between 10 and 100 micrometers.